**FOUR BIT RIPPLE CARRY ADDER**

LAB # 02



Spring 2025

CSE-308L

Digital System Design Lab

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Class Section: B

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Submitted to:

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05 March 2025

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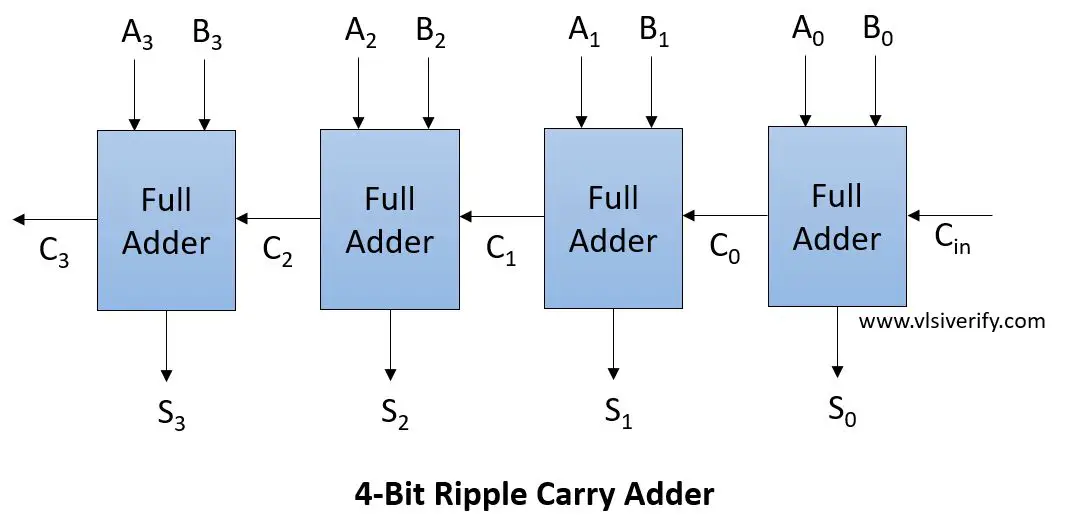
FOUR BIT RIPPLE CARRY ADDER

OBJECTIVES:

* Learn top down and bottom-up design methodologies
* Data flow level modeling
* Gate level modeling

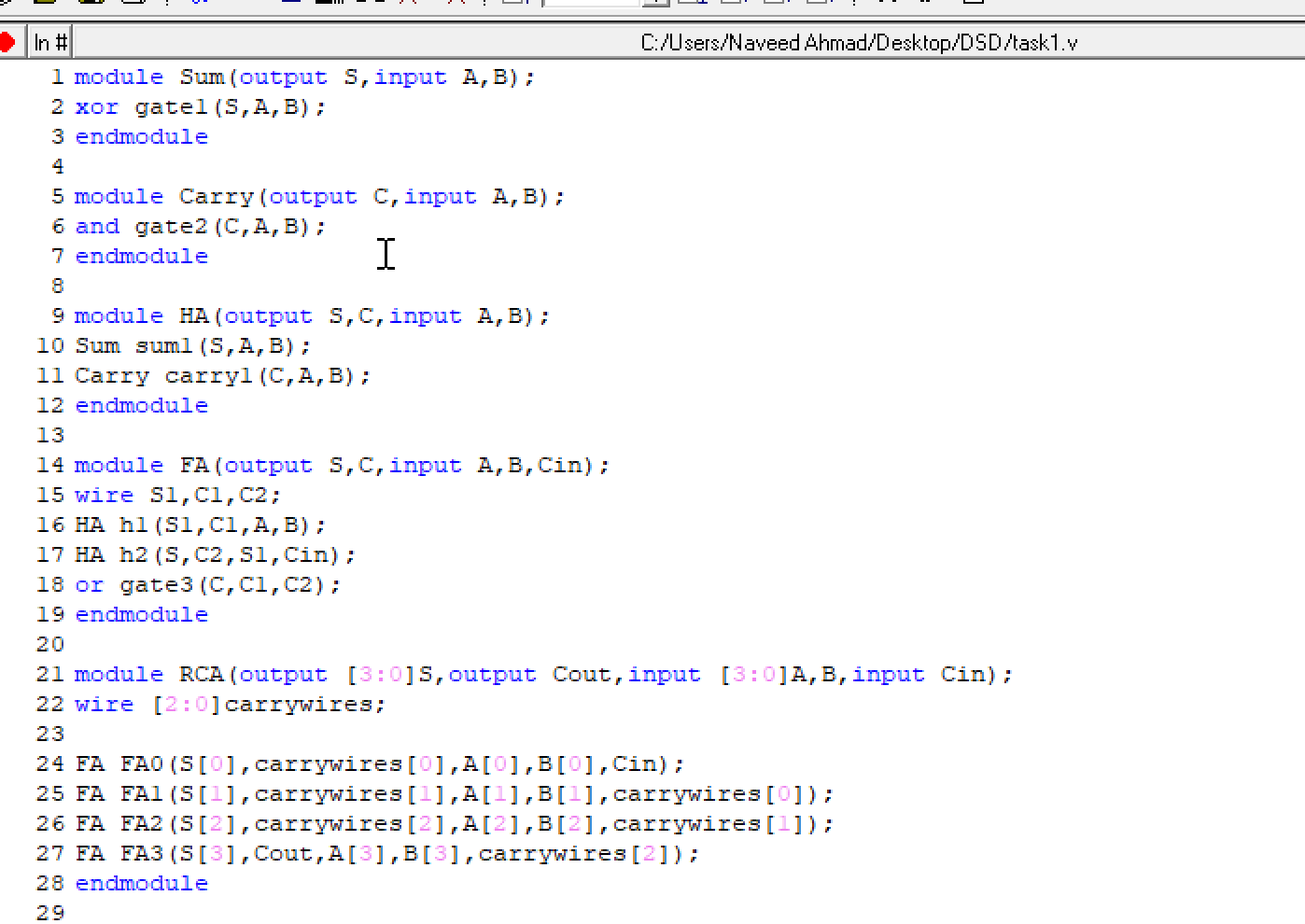
Lab Tasks:

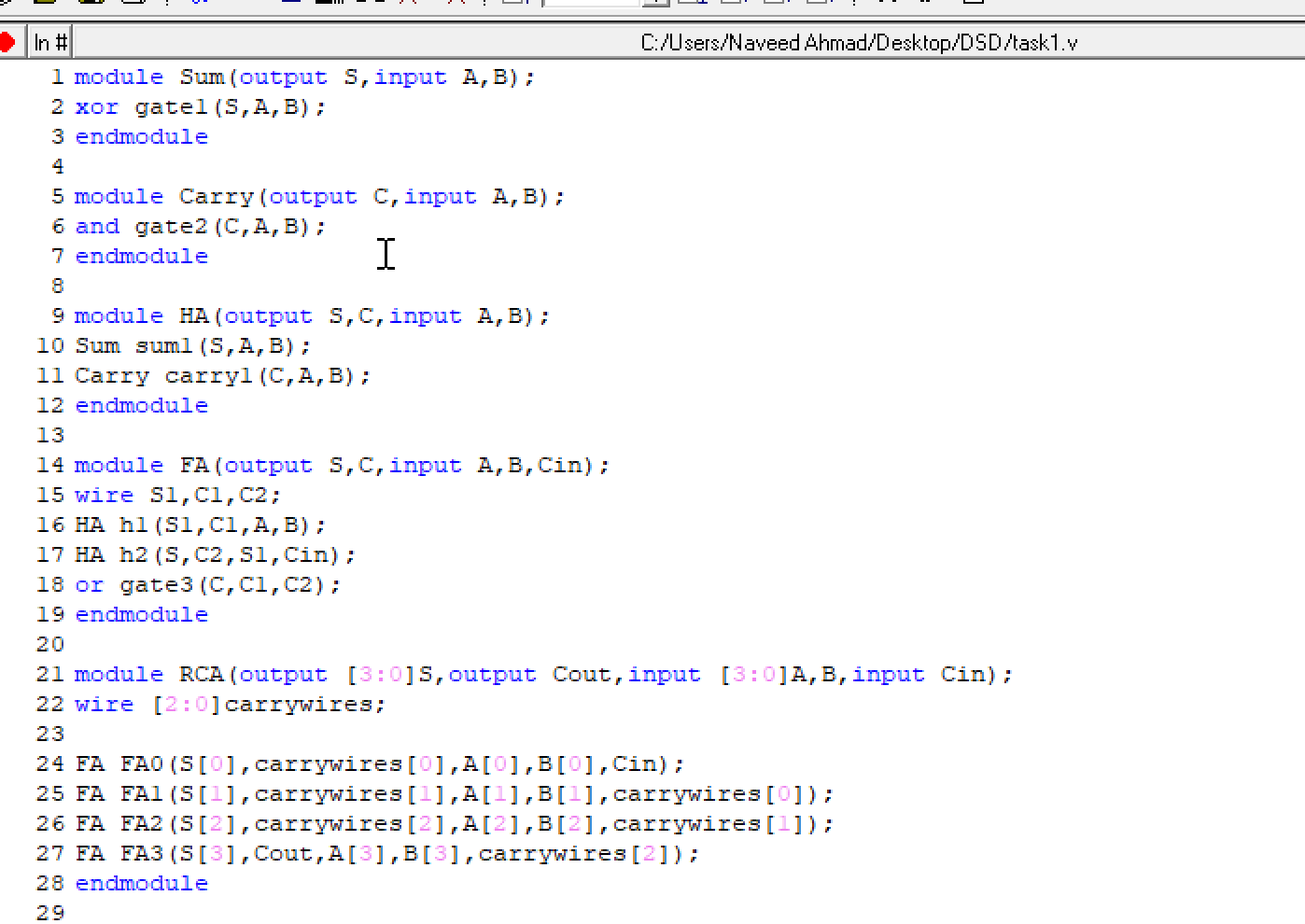
Implement a 4-bit ripple carry adder using:

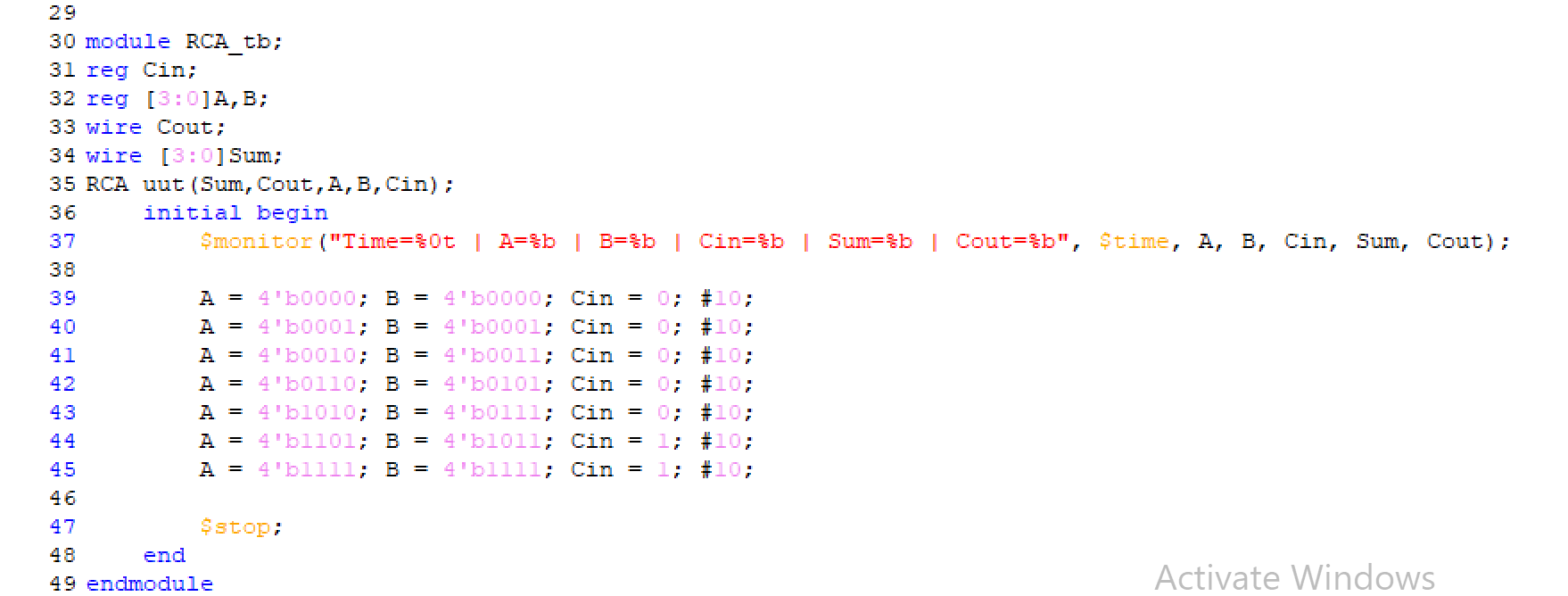


Task 1: Gate-level modeling?

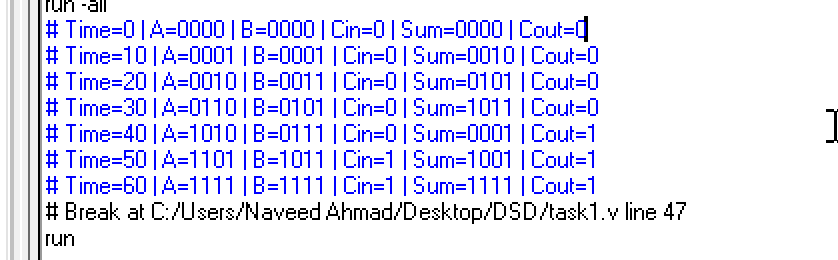
Code



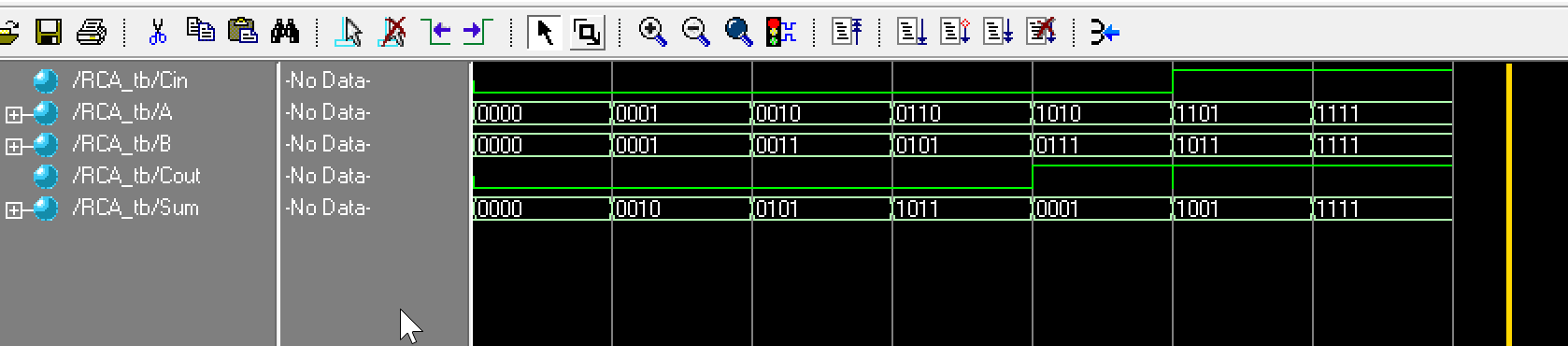




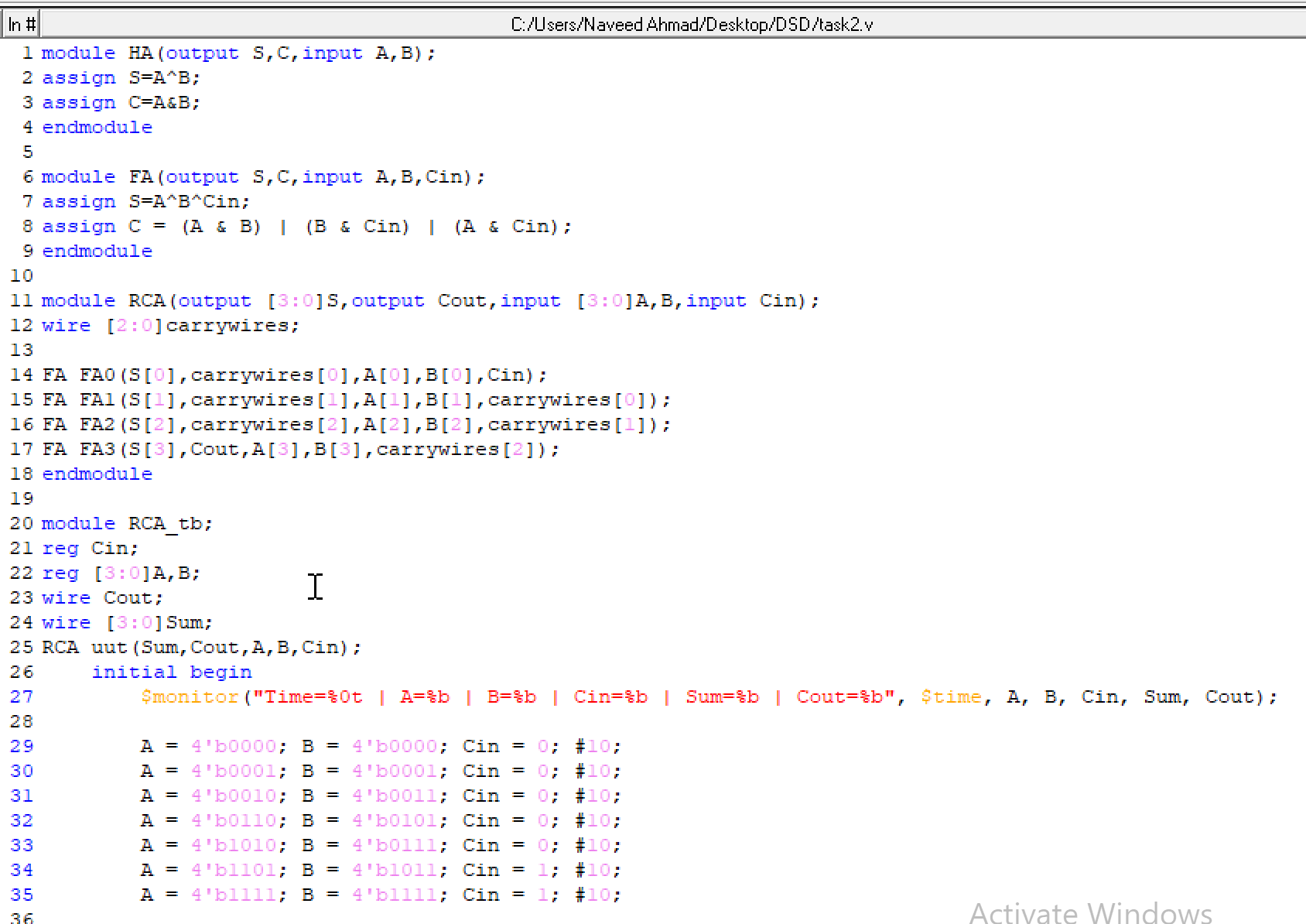
Truth table:



Output wave:

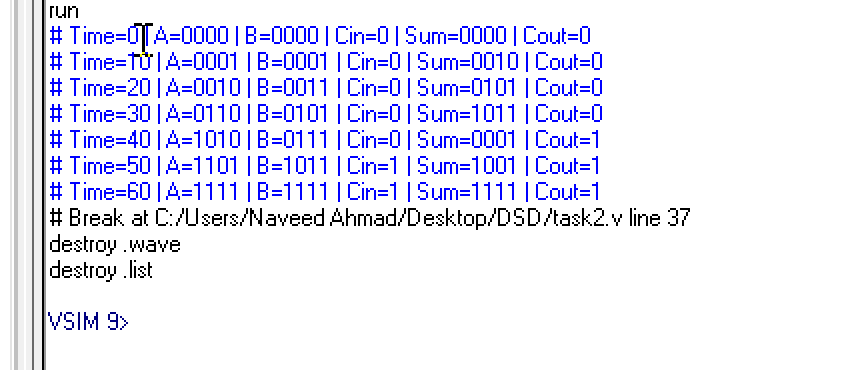


Task 2: Data-flow level modeling?

Code: 



Truth table:



Wave:

A screenshot of a computer

AI-generated content may be incorrect.